LISTING OF CLAIMS

1. (Currently Amended) A circuit, comprising:

a first ~~an~~ oscillator circuit adapted to oscillate at a predetermined frequency in response to an enable signal;

a second oscillator circuit generating an internal signal; and

an enable circuit having ~~an input and~~ an output generating the enable signal ~~coupled to the oscillator circuit~~, the ~~output of the~~ enable ~~circuit~~ signal having an inactive state upon the circuit being powered up and an active state to enable the first oscillator circuit to oscillate ~~a predetermined period of time~~ following a predetermined number of oscillations of the internal signal generated by the second oscillator circuit ~~the input of the enable circuit transitioning from the inactive state~~.

2. (Currently Amended) The circuit of claim 1, wherein the enable circuit comprises a counter operable to count the oscillations of the internal signal generated by the second oscillator circuit ~~having an enable input coupled to the input of the enable circuit and an output coupled to the output of the enable circuit~~.

3. (Currently Amended) The circuit of claim 2, wherein the second oscillator circuit ~~enable circuit further~~ comprises a ring oscillator having an output coupled to a clock input of the counter.

4. (Original) The circuit of claim 2, wherein the counter includes a control input which, when in an active state, places the counter in a predetermined state, the control input being coupled to power-on-reset circuitry.

5. (Original) The circuit of claim 4, wherein the control input is a reset input that selectively resets the counter.

6. (Currently Amended) A circuit, comprising:

an oscillator circuit adapted to oscillate at a predetermined frequency; and

an enable circuit having an input and an output coupled to the oscillator circuit, the output of the enable circuit having an inactive state upon the circuit being powered up and an active state to enable the oscillator circuit to oscillate a predetermined period of time following the input of the enable circuit transitioning from the inactive state;

~~The circuit of claim 1,~~ wherein the enable circuit comprises a ring oscillator.

7. (Currently Amended) The circuit of claim 1, wherein the first oscillator circuit comprises:

a crystal;

at least one capacitor coupled to the crystal; and

a transistor coupled across the capacitor and having a control terminal coupled to the output of the enable circuit.

8. (Currently Amended) The circuit of claim 1, further comprising:

a current source that selectively sources current to the first oscillator circuit, including at least one enable input; and

a control circuit having an input coupled to the output of the enable circuit and at least one output coupled to the at least one enable input of the current source.

9. (Currently Amended) A method for enabling an oscillator circuit to oscillate, comprising:

~~receiving a power-on-reset signal;~~

counting a certain number of clock cycles following initial power powering up of the oscillator circuit;

generating an enable signal, in response to the counting of the certain number of clock cycles, that transitions from an inactive state to an active state so as to enable the oscillator circuit to oscillate ~~, the enable signal transitions to the active state a period of time following the power-on-reset signal transitioning from a reset state~~; and

applying the enable signal to the oscillator circuit.

10. (Currently Amended) A method for enabling an oscillator circuit to oscillate, comprising:

receiving a power-on-reset signal;

generating an enable signal that transitions from an inactive state to an active state so as to enable the oscillator circuit to oscillate, the enable signal transitions to the active state a period of time following the power-on-reset signal transitioning from a reset state; and

applying the enable signal to the oscillator circuit;

~~The method of claim 9,~~ wherein the step of generating an enable signal comprises counting a number of periods of a clock signal and driving the enable signal to the active state when a predetermined number of clock periods appear on the clock signal.

11. (Original) The method of claim 10, wherein the predetermined number of clock periods are counted from a time when the power-on-reset signal transitions from the reset state.

12. (Original) The method of claim 10, wherein the step of generating an enable signal further comprises generating the clock signal.

13. (Currently Amended) A method for enabling an oscillator circuit to oscillate, comprising:

receiving a power-on-reset signal;

generating an enable signal that transitions from an inactive state to an active state so as to enable the oscillator circuit to oscillate, the enable signal transitions to the active state a period of time following the power-on-reset signal transitioning from a reset state; and

applying the enable signal to the oscillator circuit;

~~The method of claim 9,~~ wherein the oscillator circuit comprises a crystal, and the step of applying comprises shorting a terminal of the crystal to a predetermined voltage when the enable signal is in the inactive state and releasing the shorting of the terminal when the enable signal is in the active state.

14. (Currently Amended) A circuit, comprising:

an oscillator circuit capable of oscillating at a predetermined frequency; and

an enable circuit having an output coupled to the ~~crystal~~ oscillator circuit, the output of the enable circuit transitioning from an inactive state to an active state so as to enable oscillation of the oscillator circuit, the transitioning of the output happening a predetermined number of counted clock cycles ~~period of time~~ following the circuit being initially powered ~~, for enabling the oscillating the oscillator circuit to oscillate~~.

15. (Currently Amended) The circuit of claim 14, wherein the enable circuit comprises a counter for counting the predetermined number of clock cycles ~~having an output coupled to the output of the enable circuit~~.

16. (Currently Amended) The circuit of claim 15, wherein the enable circuit further comprises a ring oscillator generating the clock cycles ~~having an output coupled to a clock input of the counter~~.

17. (Original) The circuit of claim 15, wherein the counter includes a control input which selectively places the counter in a predetermined state.

18. (Original) The circuit of claim 17, wherein the control input is a reset input that selectively resets the counter.

19. (Original) The circuit of claim 17, wherein the control input receives a power-on-reset signal.

20. (Currently Amended) A circuit, comprising:

an oscillator circuit capable of oscillating at a predetermined frequency; and

an enable circuit having an output coupled to the crystal oscillator circuit, the output of the enable circuit transitioning from an inactive state to an active state a predetermined period of time following the circuit being initially powered, for enabling the oscillating the oscillator circuit to oscillate;

~~The circuit of claim 14,~~ wherein the enable circuit comprises a ring oscillator.

21. (Original) The circuit of claim 14, wherein the oscillator circuit comprises:

a crystal;

at least one capacitor coupled to the crystal; and

a transistor coupled across the capacitor and having a control terminal coupled to the output of the enable circuit.

22. (Original) The circuit of claim 14, further comprising a power-on-reset circuit, wherein the enable circuit comprises a counter having an output coupled to the output of the enable circuit and a control input used to selectively place the counter in a known state, the control input being coupled to the output of the power-on-reset circuit.

23. (Original) The circuit of claim 14, further comprising:

a current source that selectively sources current to the oscillator circuit and includes at least one enable input; and

a control circuit having an input coupled to the output of the enable circuit and at least one output coupled to the at least one enable input of the current source.

24. (Original) The circuit of claim 23, wherein the control circuit comprises a pulse generator having an input coupled to the output of the enable circuit, and a transistor coupled between nodes in the current source and having a control terminal coupled to an output of the pulse generator, the transistor being temporarily activated by the pulse generator.

25. (Currently Amended) A system, comprising:

a circuit having an oscillating signal input; and

oscillator circuitry for receiving an enable signal and generating ~~an~~ the oscillating signal ~~at an output of the oscillator circuitry, the output of the oscillator circuitry being coupled to the~~

~~circuit, the oscillating signal oscillating~~ following a predetermined number of counted clock cycles ~~period of time~~ following the received enable signal transitioning its ~~to a first logic~~ state.

26. (Currently Amended) A system, comprising:

a circuit; and

oscillator circuitry for receiving an enable signal and generating an oscillating signal at an output of the oscillator circuitry, the output of the oscillator circuitry being coupled to the circuit, the oscillating signal oscillating a predetermined period of time following the received enable signal transitioning to a first logic state;

~~The system of claim 25,~~ wherein the oscillator circuitry comprises:

a counter having a control input utilized to place the counter in a predetermined state, a clock input and an output, the control input being coupled to the enable signal; and

a crystal having a terminal coupled to the output of the counter.

27. (Original) The system of claim 26, wherein the oscillator circuitry further comprises a ring oscillator having an output coupled to the clock input of the counter.

28. (Original) The system of claim 26, wherein the oscillator circuitry further comprises a transistor having a conduction terminal coupled to the terminal of the crystal and a control terminal coupled to the output of the counter.

29. (Original) The system of claim 26, wherein the oscillator circuitry further comprises a logic inverter coupled to the crystal, and a current source for selectively providing current to the logic inverter, the current source having an enable input coupled to an output of the counter.